Modeling, Fabrication, and Characterization of Planar Inductors on YIG Substrates

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Abstract. This paper presents the design, fabrication, and characterization of micro planar inductors on a microwave magnetic material (YIG). Planar spiral inductors were designed for monolithic DC-DC converters in System-In-Package with 100 MHz switching frequency (1 W, V_{in}=3.6 V, V_{out}=1 V). A microwave magnetic substrate (YIG) serves as mechanical support and also presents a double purpose by increasing inductance value and reducing electromagnetic perturbations. This last point seems to be a critical point to improve the good behavior of a switching mode power supply. In order to obtain the optimal design for the inductor, geometrical parameters were studied using Flux2D simulator and an optimized 30 to 40 nH spiral inductor with expected 25 mΩ R_{DC}, 3 mm^2 surface area was designed. Subsequently, samples were fabricated by electroplating technique, and then tested using a vector network analyzer in the 10 MHz to 100 MHz frequency range. Results were then compared to the predicted response of simulated equivalent model.

Introduction

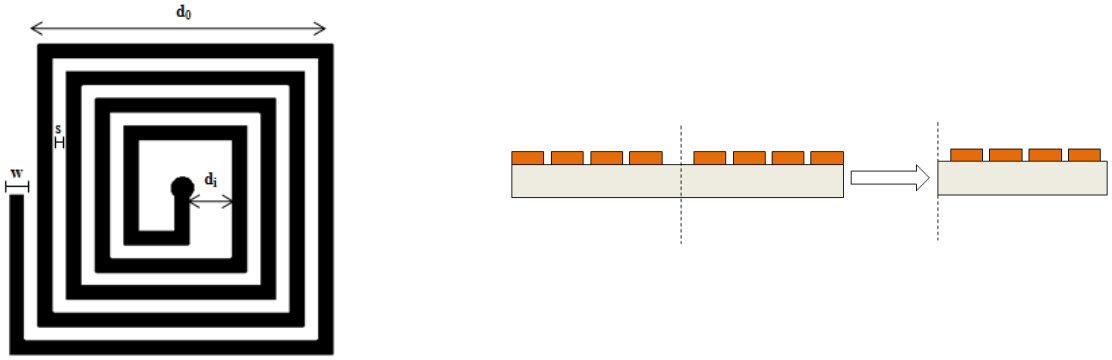
Passive components comprise the majority of chip area occupied by monolithic converters, even when the components are optimized for minimum area [1]. System-In-Package applications are facing miniaturization issues due to passive components size. The push towards higher and higher frequencies has generated much interest in novel structures for planar inductors. Therefore by increasing the switching frequency of DC-DC converters in the 10 MHz and 100 MHz frequency range, the size of filter passive components is dramatically reduced. Thus, the passive area of integration drops below the 10 mm^2 range [2].

Planar devices offer several advantages. Some of these are better thermal management, low profile, and higher power densities. Although research on planar inductors is concentrated on integrating air core inductors on silicon wafers [3,4,5], the application of YIG substrates to planar inductors enables to increase the inductance without increasing the stray capacitance between the coils and the ground plane. In our application, surface area is the key point of designing the inductor since the aim is to integrate the inductor on the top of a SMPS die in a surface area of 3mm^2. We proposed a figure of merit (MHz/mΩ.mm^2) to evaluate our inductor performance targeting the DC/DC converter application. First, we describe the design issue based on Flux2D simulator. In the second part, fabrication process using electroplating technique will be detailed. And then, experimental results and micro-fabricated inductors are shown in the last section.

Design and Simulation Results

In order to obtain the optimal design and performance for the inductor, Flux2D software, a field solver based on finite elements has been used. A very accurate numerical solution may be obtained

by using a three-dimensional finite-element simulator such as MagNet [6]. However, 3-D simulators are computationally intensive and require long run times, thus our model was studied in 2D using axial symmetric conditions as shown in Fig. 1(b). The aim of the simulations performed is to evaluate the impact of geometrical parameters of our structure on the inductance value and analyze frequency dependence of series resistance and inductance. As described in Fig. 1(a), the geometry characteristics of interest are the width of the strip *w*, the thickness of copper lines *t*, the number of turns *n*, the spacing between the turns *s*, and the inner diameter d_i. These parameters were evaluated with the spiral inductor surface area limited by 3 mm^2 which is the key point in the design of the inductor since the aim is to integrate the inductor on top of a SMPS die.



(a) (b)

Fig. 1 (a) Spiral inductor geometry, (b) Cross section of the simulated inductor model

The inductor was designed on a magnetic material (YIG) with a relative magnetic permeability μ_r = 25 [8] in our frequency range. In [7], it is demonstrated that capacitive effects between the turns of a spiral can be neglected up to 1 GHz. Skin effect is taken into consideration as it contributes to increasing series resistance of the inductor at high frequency. Since the inductor is designed for reducing current ripple, average current and resistance computed at low frequency are the main contributors to losses. In this condition, a specific Merit factor (Eq.1) taking in consideration DC resistance and inductance value was proposed to compare different models in our area of interest.

$$\mathrm{IFM} = \frac{L_{100\mathrm{MHz}}(\mathrm{nH})}{R_{DC}(\mathrm{m\Omega}) \times S(\mathrm{mm^2})}. \quad (1)$$

Simulations Guidelines

Simulations have shown that:

- YIG doubles inductance value compared to an air core inductor with the same winding and reduces electromagnetic noise which interferes with other components on the die. Moreover, simulations have also shown that YIG thickness above 200 µm has a slight effect on the inductance value.
- Copper thickness has a very small effect on inductance, but it contributes to a lower DC resistance.
- Increasing the space between the turns lowers the interwinding magnetic coupling, and thus decreases the inductance value.
- Widening the conductors reduces the inductance value, but it has an overall positive effect on Merit factor due to R_{DC} decreasing more significantly.
- Inductance value increases with the number of turns, but Merit factor remains constant. This can be explained by the fact that improvement of IFM is slowed down by the increase of the series resistance.
- Narrowing the inner diameter implies increasing the negative magnetic coupling and hence lowering the inductance value.

Simulations allowed us to evaluate our design with the optimal geometry contributing to the highest Merit factor with taking into consideration the limits of the fabrication process.

Technological process

Using the guidelines acquired through simulation analyses, we designed a planar spiral inductor of 3mm^2 surface area which was fabricated to target an inductance value of 30 to 40 nH at 100 MHz with R_{DC} as low as possible. The inductors has four turns with w = 75 µm, s = 75 µm, d_i = 200 µm, and t = 50 µm.

Fabrication process is shown in Fig. 2. A seed layer Ti 500 Å /Cu 1500 Å is deposited on the YIG substrate (a). Dry film photoresist is then laminated, and patterned (b). Next, copper lines are electroplated to mould photoresist patterns (c). Finally, the remaining dry film is removed and the seed layer is wet etched to isolate the coil turns (d).

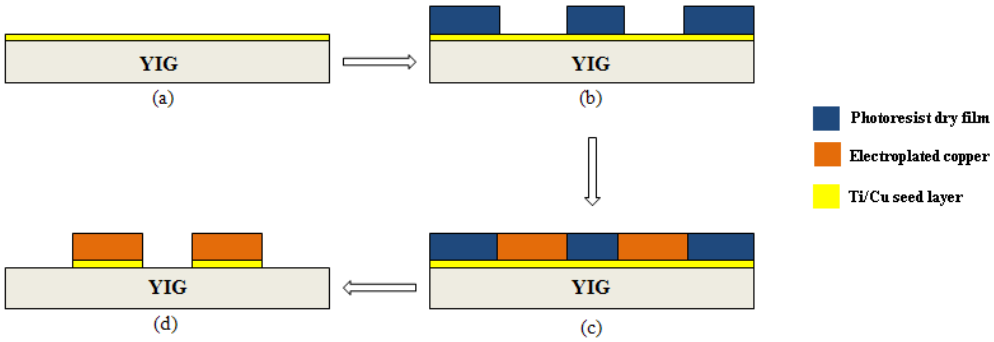
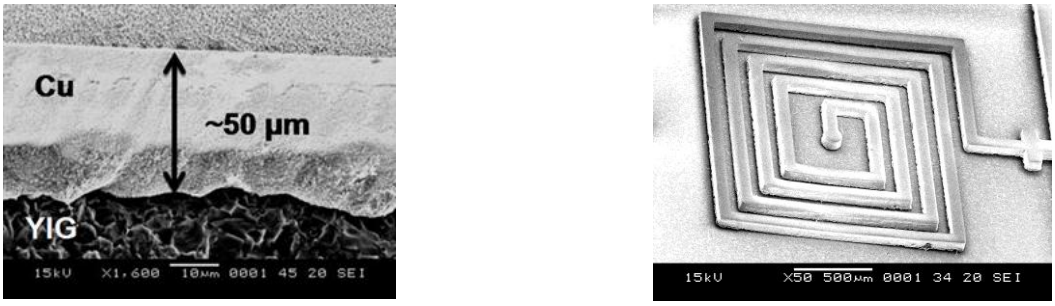


Fig. 2 Fabrication process of the spiral inductor

Copper electrodeposition is a low cost deposition technique that allowed us to achieve high aspect ratio: 75 µm in width and 50 µm in copper thickness at room temperature as shown in Fig. 3(a).



(a) (b)

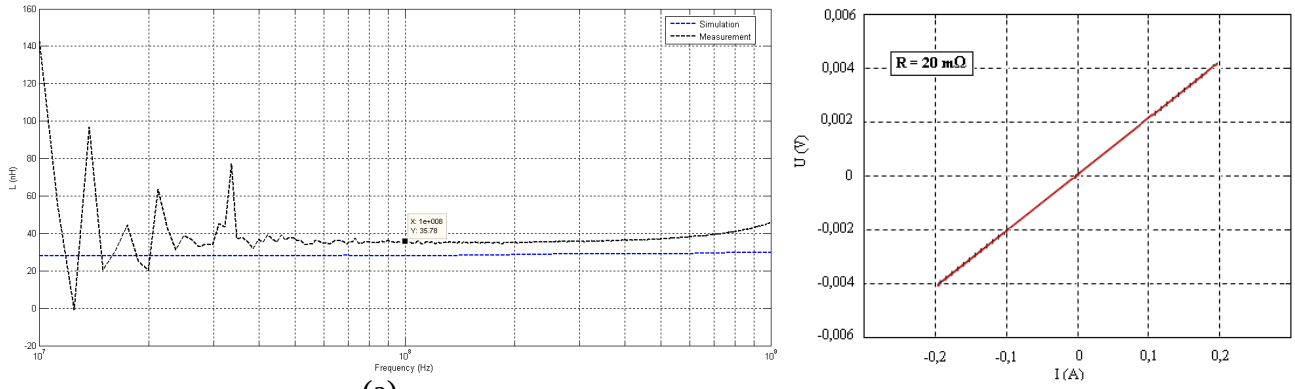
Fig. 3 SEM images of the micro-fabricated inductor

Results and Discussion

On-wafer device measurements have been carried out using Rohde & Schwarz ZVA67 Vector Network Analyzer and Cascade Microtech Air Coplanar GSG probes from 10 MHz to 1GHz. Two-port scattering parameters (S-parameters) have been measured and then changed to admittance parameters (Y-parameters). Inductance L of the spiral inductor is subsequently extracted from the resultant Y_{11} parameters after the de-embedding procedure. Its expression is given as

$$L = \frac{1}{\frac{\mathrm{Imag}[Y_{11}]}{2\times\pi\times\mathrm{Frequency}}}. \quad (2)$$

Fig. 4 (a) shows the simulated and measured inductance from 10 MHz to 1 GHz. We measured an inductance value of 35,78 nH at 100 MHz. The slight difference between the simulated and measured inductance is due to the approximations applied in the simulation process. DC resistance was also measured using SMU. We determined a value of 20 mΩ (Fig. 5). Merit factor corresponding to our application is equal to 0,6 nH/mΩ.mm^2.



(a) (b)

Fig. 4 (a) Measured and simulated inductance of the spiral inductor, (b) Measured DC resistance

Summary

In conclusion, planar spiral inductors were realized by electroplating technique. Electroplating copper lines on YIG substrate showed an improvement in the inductance value by a factor of 2 compared to an air core structure. We also reached a Merit factor of 0,6 nH/mΩ.mm^2 which is a typical value for a planar inductor that will be integrated in a monolithic DC-DC converter with 100 MHz switching frequency.

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